B1 cont'd

58.(New) A semiconductor device according to Claim 55, wherein a portion of said rear surface of said semiconductor chip is adhered to said first and second portions of said chip mounting portion, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

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59.(New) A semiconductor device according to Claim 58, wherein said semiconductor chip has a tetragonal shape, and wherein said both ends of each of said first and second portions are located at the vicinity of four corners of said semiconductor chip.

REMARKS

This Preliminary Amendment submits the following amendments and remarks for entry and consideration in the present divisional reissue application.

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES

Claims 1-14 were issued in the original patent upon which the parent reissue application of the present divisional reissue case is based. Unrelated to any prior art rejection, appropriate Claims have been amended and/or added herein to adjust a clarity and/or focus of Applicant's claimed invention. New Claims 15-59 submitted herein, which parallel reissue parent Claims 15-36 and 50-72, respectively, and have been slightly broadened/simplified by removing limitations believed unnecessary for patentability. More particularly, prior claim limitations concerning, for example, "a plurality of leads each having an inner lead portion and an outer lead portion" have

been broadened/simplified to simply "a plurality of leads." Further, prior claim limitations of "a resin member sealing...said inner lead portions" have been broadened/simplified to "a resin member sealing...at least a portion of said leads."

All amendments to Claims 1-14, and all new Claims 15-59, find full support in the patent as issued and the parent reissue application. No new matter is added.

At entry of this paper, Claims 1-59 are pending in this divisional reissue application for consideration and examination.

REQUEST FOR EXAMINER INTERVIEW PRIOR TO FIRST ACTION
AND NOTIFICATION OF INTENT TO FILE PRELIMINARY AMENDMENT

An Examiner Interview prior to first Office Action in this continuing or substitute application is respectfully requested. As stated in MPEP §713.02, "A request for an interview prior to first Office Action is ordinarily granted in continuing or substitute applications." Similarly, as stated in MPEP §706.07(b), "A request for an interview prior to first action on a continuing or substitute application should ordinarily be granted." After such Examiner Interview, Applicant may file a further Preliminary Amendment for adjusting/submitting claims which should be examined in the present divisional reissue application. The Examiner is respectfully requested to contact the attorney indicated on this paper at the local Washington, D.C. area telephone number of 703-312-6600 for the purpose of scheduling an Examiner Interview. The Examiner is thanked in advance for such considerations. Contact will also be attempted by the undersigned attorneys to schedule an Examiner Interview.

DISCLOSURE/SPECIFICATION AMENDMENTS

In the parent reissue application of the present divisional reissue case, the disclosure/specification was objected because of minor informalities. Therefore, the amendments to the specification that have been adopted in the parent reissue application are repeated in the present divisional reissue case.

Further, the specification has been amended to supply a required Notice Section indicating that more than one application has been filed for reissue of a single patent, and such Notice will be updated upon receipt of the required information by Applicant.

Any spelling, idiomatic, grammatical and/or other informality noted during any further review of the disclosure/specification will be appropriately corrected.

CLAIM FOR PRIORITY

Applicant hereby claims priority under 35 USC §119 of JP 4-320098 filed 30 November 1992 and JP 4-71116 filed 27 March 1992. The certified copies of the priority documents were submitted on 29 March 1993 in prior application Serial No. 08/038,684, which matured into U.S. Patent No. 5,637,913, the patent on which the parent reissue and the present divisional reissue cases are based. Acknowledgment of the claim for priority in this divisional reissue application is courteously solicited.

INFORMATION DISCLOSURE STATEMENT

Attached hereto are Forms PTO-1449 listing all of the references cited to or by the Office in the patented file and the parent reissue application upon which this divisional reissue application is based. In accordance with 37 CFR §§ 1.97 and 1.98,

Applicant respectfully requests return of copies of the Forms PTO-1449 bearing the Examiner's initials indicating entry and consideration of the information listed on the attached Forms PTO-1449, so that the information appears on the printed face of any reissue patent issuing on the present divisional reissue application.

In addition, attention is directed to MPEP §904, which states that, "In all continuing applications, the parent applications should be reviewed by the Examiner for pertinent prior art.", and further states that the fact of review "...should be made of record in accordance with the procedure set forth...[in]...MPEP §717.05." Any independent review by the Examiner of the prior application(s) and utilization of any necessary Form PTO-892s to ensure that all known prior application art is considered and listed on any patent issuing from the present application would be greatly appreciated by the Applicant and the undersigned.

EXAMINER INVITED TO TELEPHONE

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703-312-6600 for discussing any Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims listed above as presently being under consideration in this divisional reissue application are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

Please charge any shortage in fees necessitated by this Preliminary Amendment or divisional reissue application, including excess claim fees, to ATS&K Deposit Account No. 01-2135 (as Order No. 501.32049RV2), and credit any overpayment or excess fee thereto.

Respectfully submitted,

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ATTACHMENTS:
APPENDIX A-MARKED VERSION
Forms PTO-2038 (2)

APPENDIX A-MARKED VERSION

Paragraph at page 6, lines 31-41:

In case the aforementioned individual portions are formed by the pressing, burrs 11 are left on the back of the cut portions. Since the leadframe 1 of the present embodiment is made such that the die pad 3 has a smaller area than that of the semiconductor chip 2 to be mounted thereon, the burrs 11, if any, on the face of the die pad 3 for mounting the semiconductor chip 2 will be unable to mount the chip 2. When the die pad 3 is to be pressed, therefore, it is pressed with its chip mounting [Face] face being directed upward so that the burrs 11 may be left on the back opposed to the chip mounting face.

Paragraph at page 8, lines 46-50:

As shown in FIG. 15, moreover, slightly wider small pads (or adhesion-applied portions) 20 than the suspension leads 4 may be formed around he die pad 5 so that the adhesive [1S] 15 may be applied to the individual principal faces of the die pad 3 and the small pads 20.

IN THE CLAIMS:

1.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a

width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

6.(Once Amended) A semiconductor integrated circuit device according to [claim] Claim 5, wherein said resin member has a rectangular shape, and wherein

said [outer lead portions are extended outwardly from] plurality of leads extend in a direction of four sides of said rectangular-shaped resin member.

11.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip[,];

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;].

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

13.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said said semiconductor chip[,];

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

14.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.